Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims

1-16. (cancelled)

17. (currently amended) A high speed serial communication system, comprising:

transmission circuitry that synthesizes a first clock signal having any one of a plurality of predetermined frequencies by serializing a first predetermined sequence of first and second byte patterns, wherein said circuitry receives the contents of said first and second byte patterns in parallel, the serialization of which generates a serialized sequence that is transmitted to receiver circuitry at a serial clocking frequency, said predetermined frequency of said clock signal being a function of said serial clocking frequency and said serialized sequence; and

wherein said transmission circuitry synthesizes a second clock signal having a second predetermined frequency by serializing a second predetermined sequence of third and fourth byte patterns.

18. (currently amended) The system of claim 17, wherein said receiver circuitry receives said serialized sequence at said serial clocking frequency and derives said first clock signal by monitoring said serialized sequence for bit transitions, wherein the string of logic HIGH and LOW bits occurring between said transitions represent said predetermined frequency of said first clock signal.

19. (original) The system of claim 17, wherein said transmission circuitry comprises:

memory that stores said first and second byte patterns;

multiplexer circuitry that selects which one of said first and second byte patterns are to be serialized; and

serializer circuitry that serializes the byte patterns selected by said multiplexer circuitry.

20. (currently amended) The system of claim 19, wherein said transmission circuitry further comprises:

controller circuitry having stored therein said first predetermined sequence for instructing said multiplexer circuitry to select said first and second byte patterns according to said first predetermined sequence.

21. (original) The system of claim 17, wherein said first and second byte patterns comprise bits selected from the group consisting of logic LOW bits, logic HIGH bits, and a combination of logic LOW and HIGH bits.

22. (currently amended) The system of claims 21, wherein the bit arrangement of said first and second byte patterns are selected based on said predetermined frequency of said first clock signal.

23. (original) The system of claim 17, wherein said serialized sequence is transmitted to said receiver circuitry as a differential signal.

24. (original) The system of claim 17, wherein said predetermined frequency is a frequency existing at or below said serial clocking frequency.

25. (cancelled)

26. (currently amended) The system of claim [[25]] 17, wherein said first and second byte patterns are different than said third and ~~forth~~ fourth byte patterns.

27. (previously presented) A method for synthesizing a clock signal of a predetermined frequency, comprising:

providing a serial clocking frequency;

providing a first byte pattern and a second byte pattern, wherein the contents of said first and second byte patterns are received in parallel;

selecting a predetermined sequence of said first and second byte patterns, wherein said sequence comprises a predetermined number of said first byte pattern and a predetermined number of said second byte pattern; and

serializing said predetermined sequence according to said serial clocking frequency to generate a serialized sequence, said predetermined frequency being a function of said serialized sequence and said serialized clock signal.

28. (original) The method of claim 27, wherein said first and second byte patterns comprise bits selected from the group consisting of logic LOW bits, logic HIGH bits, and a combination of logic LOW and HIGH bits.

29. (original) The method of claim 27, further comprising transmitting said serialized sequence to receiver circuitry.

30. (original) The method of claim 29, wherein said serialized sequence is transmitted as a differential signal.

31. (cancelled)

32. (original) The method of claim 27, wherein said predetermined frequency is a frequency at or below said serial clocking frequency.

33. (original) The method of claim 27, further comprising monitoring said serialized sequence for bit transitions, wherein said transitions represent said predetermined frequency.

34. (original) The method of claim 27, further comprising:

providing a third byte pattern and a fourth byte pattern;

selecting a second sequence of said third and fourth byte patterns;

serializing said second sequence according to said serial clocking frequency to generate a second serialized sequence, said second predetermined frequency being a function of said second serialized sequence and said serialized clock signal.